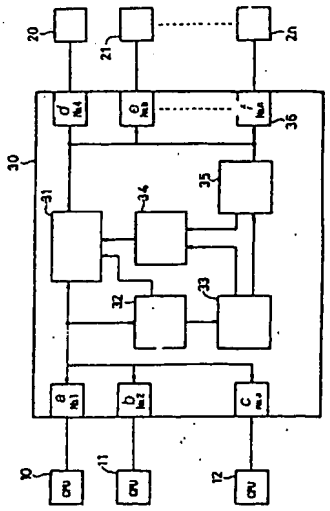
ref 2

(54) INPUT/OUTPUT CONTROL SYSTEM
(11) 5-265977 (A) (43) 15.10.1993 (19) JP
(21) Appl. No. 4-62325 (22) 18.3.1992
(71) HITACHI LTD (72) YOSHIHIKO ABE(1)
(51) Int. Cl⁵. G06F15/16,G06F13/14

PURPOSE: To improve the availability of a peripheral device by grouping plural peripheral devices, and executing input/output by selecting the arbitrary peripheral device in an unworking state in a group to which the required peripheral device belongs.

CONSTITUTION: In a controller 30, a group address discriminating part 32 discriminates whether a frame transferred from one of CPUs 10 to 12 is direct designation or group designation. Then, at the time of the group designation, the group address is sent to a group address correspondence table 33. A working state managing part 35 selects the working state of the peripheral devices 2 connected to ports 36 corresponding to the plural addresses sent from the table 33, and a port address selecting part 34 selects the unworking peripheral device 2. A data switch part 31 sends the transferred frame sent from the CPU to the port 36 corresponding to the port address sent from the port address selecting part 34.

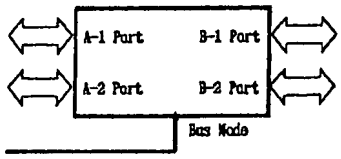


20,21,2n: peripheral device, a: port No.1, b: port No.2, c: port No.3, d: port No.4, e: port No.5, f: port No.n

(54) BUS SWITCHING TYPE MULTI-PROCESSOR SYSTEM
(11) 5-265978 (A) (43) 15.10.1993 (19) JP
(21) Appl. No. 4-59922 (22) 17.3.1992
(71) SONY CORP (72) KENICHI NAKANISHI
(51) Int. Cl⁵. G06F15/16

PURPOSE: To instantaneously execute data switching between each of processors by switching the corresponding memory of each processor by using a bus-switchboard.

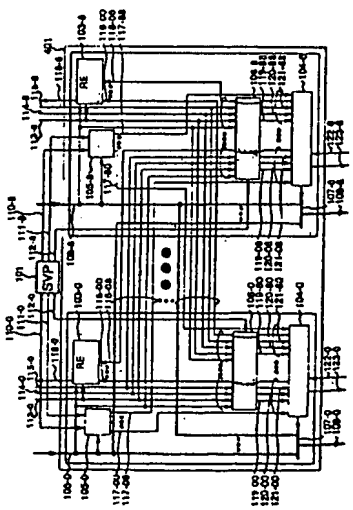
CONSTITUTION: The bus-switchboard is arranged between each processor and each data memory. The bus-switchboard switches connection between A and B in accordance with High/Low of a Bus Mode signal. At the time of Bus Mode = Low, an interval between an A-1 port and a B-1 port and the interval between an A-2 port and a B-2 port are connected. At the time of Bus Mode = High, the interval between the A-1 port and the B-2 port and the interval between the A-2 port and the B-1 port are connected. In the case that an A side is made the processor, and a B side is made the memory, as seeing from the B-1 memory, for instance, the processor to be connected is the A-1 processor at the time of Bus Mode = Low, and is the A-2 processor at the time of Bus Mode = High.



(54) PARALLEL PROCESSOR SYSTEM AND SWITCH CIRCUIT THEREFOR
(11) 5-265979 (A) (43) 15.10.1993 (19) JP
(21) Appl. No. 4-63068 (22) 19.3.1992
(71) HITACHI LTD(1) (72) SHINICHI SHUDO(3)
(51) Int. Cl⁵. G06F15/16

PURPOSE: To prevent plural broadcast packets from being transferred to one and the same processor.

CONSTITUTION: Plural split crossbar switches different in the number of input/output ports are constituted from a crossbar switch 401 by determining the transferring destination output port of the packet by adding the number of the leading port of a split crossbar switch to which a different input port belongs to a received PE number by an addition circuit 105 for every input port even if the packet of the same received PE number is inputted from the different input port. Further, by an input port selection circuit 106 provided for every output port, the output request of the packet from the input port belonging to the split crossbar switch to which that output port belongs is accepted, and the output request of the packet from the input port belonging to the other split crossbar switches is prevented from being accepted.



103: RE control circuit, 104: arbitration circuit